Quantum Transport in Ultrasmall Devices: Proceedings of a NATO Advanced Study Institute on Quantum Transport in Ultrasmall Devices, held July 17-30, 1994, in II Ciocco, Italy (Nato Science Series B:)

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The operation of semiconductor devices depends upon the use of electrical potential barriers (such as gate depletion) in controlling the carrier densities (electrons and holes) and their transport. Although a successful device design is quite complicated and involves many aspects, the device engineering is mostly to devise a "best" device design by defIning optimal device structures and manipulating impurity profIles to obtain optimal control of the carrier flow through the device. This becomes increasingly diffIcult as the device scale becomes smaller and smaller. Since the introduction of integrated circuits, the number of individual transistors on a single chip has doubled approximately every three years. As the number of devices has grown, the critical dimension of the smallest feature, such as a gate length (which is related to the transport length defIning the channel), has consequently declined. The reduction of this design rule proceeds approximately by a factor of 1. 4 each generation, which means we will be using 0. 1-0. 15). lm rules for the 4 Gb chips a decade from now. If we continue this extrapolation, current technology will require 30 nm design rules, and a cell 3 2 size < 10 nm , for a 1Tb memory chip by the year 2020. New problems keep hindering the high-performance requirement. Well-known, but older, problems include hot carrier effects, short-channel effects, etc. A potential problem, which illustrates the need for quantum transport, is caused by impurity fluctuations.

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